

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



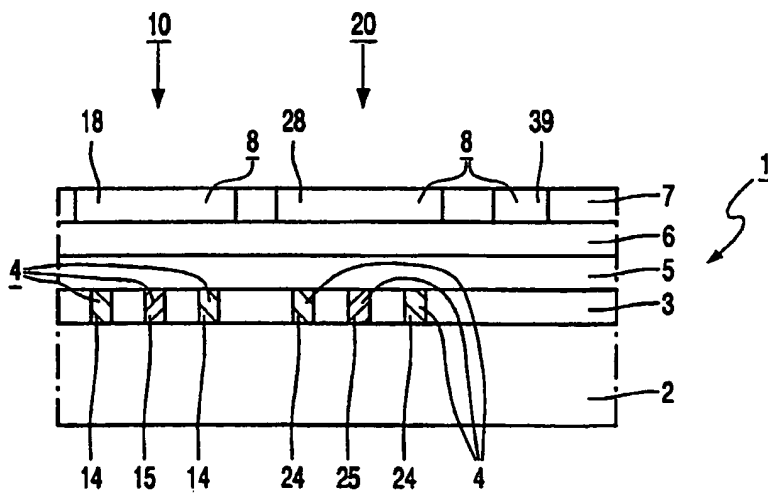
(43) International Publication Date
19 April 2001 (19.04.2001)

PCT

(10) International Publication Number
WO 01/27998 A1

- (51) International Patent Classification⁷: H01L 27/088, 51/20, 27/02 (72) Inventor: HART, Cornelis, M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (21) International Application Number: PCT/EP00/09609 (74) Agent: DUIJVESTIJN, Adrianus, J.; Internationaal Octroibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (22) International Filing Date:
28 September 2000 (28.09.2000) (81) Designated State (*national*): JP.
- (25) Filing Language: English (84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
- (26) Publication Language: English
- (30) Priority Data: 99203334.0 11 October 1999 (11.10.1999) EP Published:
— With international search report.
- (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: INTEGRATED CIRCUIT



(57) Abstract: The integrated circuit (1) suppresses leakage currents, which usually take place between neighboring transistors (10, 20) through the unpatterned semiconductor layer (5). In its first layer (3), the circuit (10) comprises electrically conductive tracks (4) which are in contact with the semiconductor layer (5), some of which tracks (4) are in use as source and drain electrodes (14, 15, 24, 25) and are preferably fork-shaped and interdigitated. The suppression of leakage currents is achieved by putting neighboring electrodes (14, 24) in different transistors (10, 20) at the same voltage and by excluding the presence of any other electrically conductive tracks between those neighboring electrodes (14, 24). Interconnect lines (39) carrying input or output signals are positioned in a second layer (7) as much as possible, which second layer (7) comprises electrically conductive tracks (8) and is not in contact with the semiconductor layer (5). The integrated circuit (1) of the invention is very well fitted to contain arrays of NAND structures.

WO 01/27998 A1